Amendments to and listing of the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

1-7. (Canceled)

8. An integrated circuit device receiving signals from a signal pad, comprising at least one substrate-biased silicon diode responsive to the signals from the signal pad for providing electrostatic discharge protection.

9. The integrated circuit device claimed in claim 8, wherein the at least one substrate-biased silicon diode includes one or more serially coupled substrate-biased silicon diodes.

10. The integrated circuit device as claimed in claim 8, wherein the at least one substrate-biased silicon diode includes a p-type polysilicon portion, an n-type polysilicon portion and a center polysilicon portion disposed between and contiguous with the p-type and n-type polysilicon portions.

11-14. (Canceled)

15. The integrated circuit device as claimed in claim 8, wherein the at least one substrate-biased silicon diode includes a p-portion and an n-portion, and wherein the signal pad is coupled to the p-portion of the at least one substrate-biased silicon diode.

16. The integrated circuit device as claimed in claim 8, further comprising a detection circuit for detecting the signals from the signal pad and providing a bias voltage to the at least one substrate-biased silicon diode.

17. The integrated circuit device as claimed in claim 8, wherein the signals from the signal pad are electrostatic pulses.

18. The integrated circuit device as claimed in claim 16, wherein the detection circuit comprises a resistor-capacitor circuit having a delay constant longer than the duration of the signals from the signal pad.

19. The integrated circuit device as claimed in claim 16, wherein the detection circuit comprises a resistor-capacitor circuit coupled in parallel to a transistor network.

20. The integrated circuit device as claimed in claim 16, wherein the detection circuit includes a first transistor, a second transistor, and a resistor-capacitor circuit, and wherein a gate of the first transistor is coupled to a gate of the second transistor and the resistor-capacitor circuit.

21. The integrated circuit device as claimed in claim 20, wherein a drain of the first transistor and a drain of the second transistor are coupled to a substrate of the at least one substrate-biased silicon diode to provide a bias voltage.

22. The integrated circuit device as claimed in claim 20, wherein a source of the first transistor is coupled to a V_{DD} signal and a source of the second transistor is coupled to a V_{SS} signal.

23. An integrated circuit device receiving signals from a signal pad, comprising:
a first plurality of serially coupled substrate-biased silicon diodes responsive to the signals from the signal pad for providing electrostatic discharge protection from the signals, each of the first plurality of substrate-biased silicon diodes including a p-portion and an n-portion;
a second plurality of serially coupled substrate-biased silicon diodes responsive to the signals from the signal pad for providing electrostatic discharge protection from the signals, each of the second plurality of substrate-biased silicon diodes including a p-portion and an n-portion; and

a detection circuit for detecting signals from the signal pad and providing a bias voltage to the first and second plurality of substrate-biased silicon diodes,

wherein the signal pad is coupled to the p-portion of one of the first plurality of substrate-biased silicon diodes and the n-portion of one of the second plurality of the substrate-biased silicon diodes.

24. The integrated circuit device as claimed in claim 23, wherein the detection circuit comprises a first transistor; a second transistor, and a resistor-capacitor network, and wherein a gate of the first transistor is coupled to a gate of the second transistor and the resistor-capacitor circuit.

25. The integrated circuit device as claimed in claim 24, wherein a drain of the first transistor and a drain of the second transistor are coupled to a substrate of the first and second plurality of substrate-biased silicon diodes to provide a bias voltage to the first and second plurality of substrate-biased silicon diodes.

26. An integrated circuit device, comprising
a semiconductor substrate;
an insulator layer disposed over the semiconductor substrate;
a silicon layer disposed over the insulator layer, including
a first isolation structure formed inside the silicon layer, and
a second isolation structure formed inside the silicon layer and spaced apart from the first isolation structure;
a dielectric layer disposed over the silicon layer; and
a layer of silicon, disposed over the dielectric layer, including a p-type portion, an n-type portion and a center portion disposed between and contiguous with the p-type and n-type portions.

27. The integrated circuit device as claimed in claim 26, wherein the center portion of the layer of silicon overlaps a portion of the silicon layer between the first and second isolation structures.

28. The integrated circuit device as claimed in claim 26, wherein the portion of the silicon layer between the first and second isolation structures is biased to provide electrostatic discharge protection.

29. A silicon-on-insulator circuit device receiving signals from a signal pad, comprising at least one base-biased silicon diode, responsive to the signals from the signal pad, for providing electrostatic discharge protection.

30. The silicon-on-insulator circuit device as claimed in claim 29, wherein each of the at least one base-biased silicon diodes includes a p-type polysilicon portion, an n-type polysilicon portion and a center polysilicon portion disposed between and contiguous with the p-type and n-type polysilicon portions.

31. The silicon-on-insulator circuit device as claimed in claim 29, wherein the silicon-on-insulator circuit device is biased to control the at least one base-biased silicon diode.

32. An integrated circuit device receiving signals from a signal pad, comprising one or more serially coupled base-biased silicon diodes, responsive to the signals from the signal pad, for providing electrostatic discharge protection.

33. The integrated circuit device as claimed in claim 32, further comprising a detection circuit for detecting signals from the signal pad and providing a bias voltage to the one or more base-biased silicon diodes, wherein the detection circuit comprises a resistor-capacitor network coupled in parallel to a transistor network.

34. The integrated circuit device as claimed in claim 33, wherein the transistor network includes a first transistor and a second transistor, and wherein a gate of the first transistor is coupled to a

gate of the second transistor and the resistor-capacitor network, and wherein a drain of the first transistor and a drain of the second transistor are coupled to a base of the one or more base-biased silicon diodes to provide a bias voltage.

35-51. (Canceled)